

2013 Illinois Symposium on Parallelism: Current State of the Field and the Future

Please join us at the University of Illinois at Urbana-Champaign this September 10 and 11 for the 2013 Illinois Symposium on Parallelism: Current State of the Field and the Future.

This symposium offers participants the opportunity to reflect on what parallelism research has accomplished over the last 5+ years and what challenges remain for this decade and beyond. The topics include applications, programming models and languages, compilers, tools, and architecture.

The following leading researchers will give keynotes at the symposium:

- **Dr. Tilak Agerwala**, Vice President of Systems at IBM Research
- **Prof. Arvind**, Johnson Professor of Computer Science and Engineering at the Massachusetts Institute of Technology
- **Dr. James Larus**, Principal Researcher at Microsoft Research
- **Prof. Keshav Pingali**, W.A. "Tex" Moncrief Chair of Grid and Distributed Computing at the University of Texas at Austin
- **Prof. Kunle Olukotun**, Professor of Electrical Engineering and Computer Science at Stanford University
- **Dr. Burton Smith**, Technical Fellow at Microsoft Corporation

Other guest speakers will be announced on the symposium website as they are confirmed. Many distinguished faculty from the University of Illinois will also present their research. We expect wide participation from both academia and industry.

This event is free. Attendance at the Illinois Symposium on Parallelism is free. Meals on both days of the symposium will be provided. However, all lodging and travel expenses are the responsibility of the attendee.

Registration is limited. The size of the symposium is limited to the first 70 registrants. Please register early to secure your space. Registration closes when the 70-participant limit has been reached, or on August 16.

Please see the 2013 Illinois Symposium on Parallelism website (<http://i2pc.cs.illinois.edu/parworkshop.html>) for a tentative schedule; information about lodging, meals, and travel to the University of Illinois; and registration information!

Questions? Contact the Illinois-Intel Parallelism Center at mosfar2@illinois.edu.

Josep Torrellas, Illinois Intel Parallelism Center (I2PC) Director

About The Universal Parallel Computing Research Center (UPCRC) and The Illinois Intel Parallelism Center (I2PC)

UPCRC and I2PC are partnerships between the University of Illinois at Urbana-Champaign and its corporate sponsors, the Intel and Microsoft corporations. Since their inception in 2008 and 2011, the centers have been progressing at their goal of “*Making Parallelism Easy*”. Their 19 faculty have produced a large number of visible contributions, which include:

- The *AvaScholar* framework of parallel primitives for graphics, visual computing, and tele-immersive environments to support remote instruction and education. The framework includes techniques to accelerate stereo reconstruction, emotion recognition, and the parallel construction and query of high-dimensional k-D trees.
- A *Pattern Language* for parallel programming that makes it easier to learn parallel programming, and to specify and evaluate parallel systems. The language includes patterns about algorithms that are often parallelized, as well as strategies for parallelizing algorithms and low-level patterns for structuring and controlling parallelism.
- A set of widely acclaimed interactive *Refactoring Tools* that parallelize programs by rewriting the code to use parallel libraries. These tools ship with the official release of development environments used by millions of Java programmers. The tools relieve the programmer from performing non-trivial safety analysis, and from rewriting the code.
- The *Hierarchical Tiled Arrays (HTA)* programming model, which succinctly expresses data localities for numerical and non-numerical codes. This high-level notation is programmer-friendly, while enabling efficient mapping of computation to processor clusters and data-parallel functional units.
- The *Deterministic Parallel Java (DPJ)* programming model for determinism-by-default, and its C++ counterpart, Annotations for Safe Parallelism (ASP). This project shows that an annotation system can provide strong correctness guarantees and still be very expressive. ASP is being tested for large industrial applications.
- The *Adrenaline Web Browser* and operating system, which is built from the ground up for parallelism and security. This system decomposes web content as mostly-independent mini pages that are processed in parallel. The browser’s secure core has been verified with formal methods.
- New advances in the testing and verification of parallel programs. Testing improvements include new forms of Mutation Testing and Regression Testing. An inference framework takes code annotations and infers effects and code regions using optimized solvers.
- The *QuickRec Prototype* for recording and deterministically replaying multithreaded programs in multicores. This Linux-supported FPGA prototype is likely to change the way tools for debugging and security will be built. This project also includes a suite of novel techniques for data race, atomicity violation, and sequential consistency violation detection.
- Three novel multiprocessor computer architectures that challenge existing tenets. The *Bulk Architecture* places programmability and usability as first-class principles, while retaining performance with new structures such as atomic blocks and signatures. The *DeNovo Architecture* exploits disciplined programming practices in a “have-your-cake-and-eat-it-too” approach for complexity, energy, and performance scalability. The *Rigel Architecture* streamlines the processor and cache hierarchy of a many-core for energy efficiency, delivering a superb platform for visual computing