I2PC

Illinois-Intel Parallelism Center

Distinguished Speaker Series

Andrew Chien

University of Chicago

Technology Scaling and the Future of Microprocessors: The 10x10 Approach

Thursday, February 9, 2012

4 - 5 PM CST

3405 Siebel Center

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Abstract

In the waning days of Moore's Law, Dennard scaling (density, speed, and energy) has given way density scaling with incremental improvements in transistor speed and energy. In response to energy-constraints, architects are pursuing two main approaches – parallelism (multicore CPU, GPU) and heterogeneity (accelerators, SoC) – with major challenges in programmability. While thousands of papers have been written on parallel programming, there has been little research on how to balance programmability with the energy-performance benefits of customization.

We are pursuing a new paradigm, "10x10",which enables systematic exploration of applications, programmability, and customization in a new model of general-purpose computer architecture – federated accelerators. 10x10 moves beyond the general purpose architecture implementation paradigm (90/10 optimization) by divides workloads into clusters, and systematically exploits customization separately for each cluster in a federated accelerators architecture. We call this new paradigm "10x10" because it partitions application workloads and optimizes for 10 different 10% cases, not a monolithic 90/10.

We are applying 10x10 a range of general-purpose workloads and DOE Science applications. Research challenges include how to cluster workloads, architect programmable accelerators, federate accelerators, and program them effectively. We will present the 10x10 paradigm, and initial results. The ultimate goal is to enable stable perspective on application clusters and requirements, and accelerators that enables long-term programmability and a predictable

roadmap of computer architectures.

Bio

Dr. Andrew A. Chien is the William Eckhardt Professor in Computer Science and Senior Fellow in the Computation Institute at the University of Chicago, and Senior Computer Scientist at the Argonne National Laboratory. Dr. Chien served as Vice President of Research at Intel Corporation, leading long-range and "disruptive technologies" research at Intel Research. At Intel, he also led Intel's external research programs, including government and higher education engagements. In this role, Chien launched imaginative new efforts in robotics, wireless power, sensing and perception, nucleic acid sequencing, networking, cloud, and ethnography. Working with external partners, Chien was instrumental in creation of the Universal Parallel Computing Research Centers (UPCRC) focused on parallel software, the Open Cirrus Consortium focused on Cloud computing, and Intel's Exascale Research program.

For more than 20 years, Chien has been a global research and education leader, and an active researcher in parallel computing, computer architecture, programming languages, networking, clusters, grids, and cloud computing. Previous academic positions include the SAIC Chair Professor in Computer Science and Engineering, and founding Director of the Center for Networked Systems at the University of California at San Diego. While at UCSD, he also founded Entropia, a widely-known Internet Grid computing startup.From 1990 to 1998, Chien was a Professor of Computer Science at the University of Illinois at Urbana-Champaign with joint appointments at the National Center for Supercomputing Applications (NCSA) where he was a research leader for parallel computing software and hardware, and developed the well-known Fast Messages, HPVM, and Windows NT Supercluster systems.

Dr. Chien is a Fellow of the American Association for Advancement of Science (AAAS), Fellow of the Association for Computing Machinery (ACM), Fellow of Institute of Electrical and Electronics Engineers (IEEE), and has published over 130 technical papers. Chien served on the Board of Directors for the Computing Research Association (CRA), Advisory Board of the National Science Foundation's Computing and Information Science and Engineering (CISE) Directorate, and is currently on the Editorial Board of the Communications of the Association for Computing Machinery (CACM). Chien received his Bachelor's in electrical engineering, Master's and Ph.D. in computer science from the Massachusetts Institute of Technology.

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