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Distinguished Speaker Series

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University of Illinois

BulkSMT: Designing SMT Processors for Atomic-Block Execution

Thursday, December 8, 2011

4 - 5 PM CST

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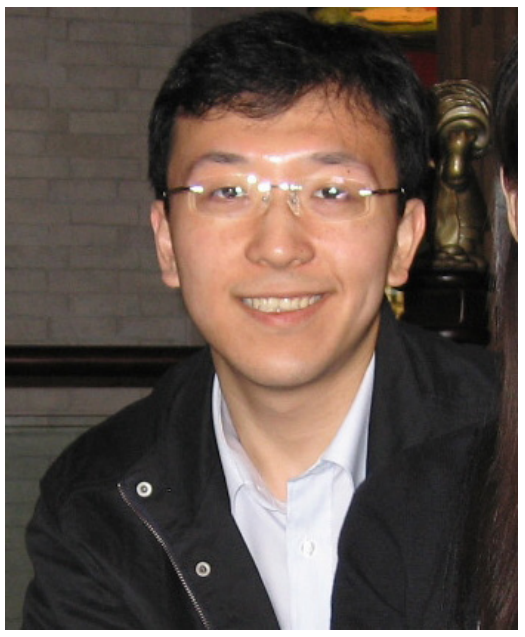

Abstract

Multiprocessor architectures that continuously execute atomic blocks of instructions can improve performance and software productivity. However, all of the proposals for such architectures assume single-context cores as their building blocks --- rather than the widely-used Simultaneous Multithreading (SMT) cores. As a result, they are effectively wasting hardware resources.

This paper presents the first SMT design that supports continuous atomic-block (or transactional) execution of its contexts. Our design, called BulkSMT, can be used either in a single-core platform or in a multi-core of SMTs.

We present a set of BulkSMT configurations with different cost and performance. We also describe the architectural primitives that enable atomic-block execution in an SMT core and in a multicore of SMTs. Our results, based on simulations of SPLASH-2 and PARSEC codes, show that BulkSMT supports atomic-block execution cost-effectively. In a 4-core multicore with eager atomic-block execution, BulkSMT reduces the execution time of the applications by an average of 26% compared to running on single-context cores.

Bio

Xuehai Qian is a PhD student in computer science at the University of Illinois at Urbana-Champaign. He works with Prof. Josep Torrellas. His research lies within the fields of cache coherence and memory models for multi- or many-core. He is currently focusing on the scalable and efficient architecture for improved programmability. He received his bachelor's degree in computer engineering from Beihang University, and his master's degree in computer science from Institute of Computing Technology (ICT), Chinese Academy of Sciences. This particular work has been accepted in HPCA, 2012.

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