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Illinois-Intel Parallelism Center

Distinguished Speaker Series

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Improving Permeability in System Architecture

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4 - 5 PM

Abstract

Hardware complexity has outpaced software development by a wide margin. Long gone are the days where well written applications and compilers could extract every drop of performance in a computing platform. Software developers are faced with the daunting task of parallelizing their applications using archaic tools that have not kept pace with hardware. Further, programmers attempting to utilize performance of specialized hardware must become proficient using hybrid environments like OpenCL.

The principal of hardware/software codesign is often cited as the panacea for closing the complexity gap and improving programmer productivity. While conceptually simple, codesign is not well defined and does not necessarily lead to systems that lend them to higher productivity. The concept of improving permeability through the hardware/software barrier is introduced as a technique to reduce overall system architecture complexity.

In this talk I will explore tradeoffs that can move specific functions from software to hardware, both for productivity and for efficiency. I will also look at examples where moving a function from hardware to software improved flexibility without compromising efficiency. Using recent product experience, we will discuss the software interfaces to hardware functions and attempt to make sense of hardware/software codesign with heterogeneous hardware.

Bio

Doug Carmean is an Intel Fellow and Researcher At Large at Intel Labs.

He is responsible for creating the vision and concept for a fully programmable graphics pipeline based on IA processors that supports highly visual and parallel workloads. Carmean led the team that founded a new group at Intel to define, build and productize products from an architecture that targets the high-end discrete graphics business. He is responsible for growing the development of Larrabee from an early concept to a core piece of Intel's graphics strategy. Carmean enlisted and included key industry software developers in Larrabee's definition to ensure a compelling product.

Since joining Intel in 1989, he has held several key roles and provided leadership in Intel's microprocessor architecture development and product roadmap. As Nehalem's first chief architect, a next-generation x86 flagship processor, he led the team during the early phases of architecture definition. Prior to this position, he was a principal architect for the Pentium 4 processor where he completed the memory cluster and power architecture definition including algorithms, structures and overall functionality.

Carmean holds more than 25 patents and many pending in processor architecture and implementation, memory subsystems and low power design. He has published more than a dozen technical papers. Doug enjoys fast cars, Canadian bicycles and scary, Italian motorcycles.

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