I2PC

Illinois-Intel Parallelism Center

Distinguished Speaker Series

Michael Voss

Intel Corporation

The Intel® Threading Building Blocks Flow Graph

Thursday, November 10, 2011

4 - 5 PM CST

3405 Siebel Center

Abstract

Many applications can be naturally expressed as computational graphs, where vertices represent computations and the edges express either ordering relationships or the passing of data between these computations. Computational graphs appear across many domains including digital content creation, gaming, finance, mobile computing and technical computing. In this talk, I will present a new feature in the Intel® Threading Building Blocks (Intel® TBB) library that allows users to easily express and execute parallel computational graphs. Intel TBB is a widely used, award-winning C++ template library for creating reliable, portable, and scalable shared-memory parallel applications. The Intel TBB flow graph leverages the library's task scheduler to create computational graphs that compose with the tasks and generic parallel algorithms provided by the library, allowing users to easily create hierarchical applications with nested parallelism.

After a brief introduction to the Intel® Threading Building Blocks library, I will present a overview of the new flow graph feature, describing the graph object, its node types and edges. I will then present examples of flow graphs including a dependency graph that performs a blocked wave-front computation across a matrix, an image processing application that performs feature recognition, and an implementation of the dining philosophers problem. I will also compare the new flow graph with other existing features in Intel TBB: directed acyclic graphs of tasks and the pipeline class. I will conclude with a summary and pointers to additional information about the flow graph and other new features in Intel® Threading Building Blocks 4.0.

Bio

Michael Voss is a Software Architect in Technical Computing, Analyzers and Runtimes at Intel. He is one of the lead developers of Intel® Threading Building Blocks (Intel® TBB) and the architect of the Intel TBB flow graph. Prior to joining Intel in 2005, he was an Assistant Professor at the Edward S. Rogers Sr. Department of Electrical and Computer Engineering at the University of Toronto. He received his Ph.D. in Electrical Engineering from Purdue University in 2001. He interests include parallel computing, adaptive program optimization, and optimizing compilers.

For more information about I2PC research, education, and activities, visit:
i2pc.cs.illinois.edu

Attend this talk remotely at:
media.cs.illinois.edu/live/I2PClive.asx

A chat interface has been set up for questions:
i2pc.cs.illinois.edu/chat

ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN